WHAT IS CLAIMED IS:

1. A MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions,

wherein the top surfaces of said source/drain regions formed on said semiconductor substrate are arranged toward said gate electrode from a reference plane of a channel plane in said semiconductor substrate, the top surfaces of said source/drain regions are arranged toward said channel plane from a reference plane of an interface between a gate insulator film formed on said channel plane and said gate electrode, and a dielectric constant of said gate insulator film is higher than that of silicon oxide.

2. A MIS transistor as set forth in claim 1, wherein a groove is formed in the top surface of said semiconductor substrate and has a bottom surface serving as said channel plane, said gate insulator film being formed in an opening of said groove via a protective film, said gate electrode being arranged on the top of said gate insulator film, said source/drain regions being arranged on both sides of said channel plane, so that a predetermined relationship between the top surfaces of said source/drain regions, said channel plane and said interface is established.

3. A MIS transistor as set forth in claim 1, wherein the top surfaces of said source/drain regions laminated in places which sandwich said channel plane on said semiconductor substrate therebetween is arranged toward said gate electrode from a reference plane of said channel plane, and the top surfaces of said source/drain regions are arranged toward said channel plane from a reference plane of said interface between said gate insulator film formed on said channel plane via a protective film and said gate electrode.

4. A MIS transistor as set forth in claim 1, wherein the top surfaces of said source/drain regions provided so as to sandwich

said channel plane therebetween is elevated from said channel plane to be arranged toward said gate electrode, and the top surfaces of said source/drain regions have a substantially flat surface having a level which is elevated and arranged toward said gate electrode, and an inclined surface which is inclined from said level of said flat surface to a level of said channel plane.

5. A MIS transistor as set forth in claim 4, wherein said gate electrode surrounded by said gate insulator film provided on the upper side of said channel plane has a cross section of a T shape, the lower side of which is tapered via a step portion.

6. A MIS transistor as set forth in claim 1, wherein said gate electrode surrounded by said gate insulator film provided on the upper side of said channel plane has a cross section of a T shape, the lower side of which is tapered via a step portion.

7. A MIS transistor as set forth in claim 1, wherein said gate insulator film includes a metal oxide film.

8. A MIS transistor as set forth in claim 7, wherein said metal oxide film includes any one of titanium oxide film, aluminum oxide film and tantalum oxide film.

9. A MIS transistor as set forth in claim 1, wherein said gate insulator film has a predetermined dielectric constant higher than that of an aluminum oxide film.

10. A MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions,

wherein the top surfaces of said source/drain regions provided so as to sandwich said channel plane therebetween is elevated from said channel plane to be arranged toward said gate electrode, and the top surfaces of said source/drain regions have a substantially flat surface having a level which is elevated and arranged toward said gate electrode, and an inclined surface which is inclined from said level of said flat surface to a level

of said channel plane; and

wherein said gate electrode surrounded by said gate insulator film provided on the upper side of said channel plane has a cross section of a T shape, the lower side of which is tapered via a step portion.

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11. A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising the steps of:

selectively forming an oxide film on said semiconductor substrate;

using the selectively formed oxide film as a mask to carry out etching to form a groove;

laminating a semiconductor layer in said groove to polish the top surfaces of said oxide film and said semiconductor film, and thereafter, removing said oxide film;

using said semiconductor film as a mask to diffuse an impurity in the surface of said semiconductor substrate to form a grooved impurity diffusion region including the bottom of said groove;

arranging a gate insulator film of a high dielectric film in a groove portion of said grooved impurity diffusion region so that the top surface of said gate insulator film is arranged farther from said semiconductor substrate than the top surface of said impurity diffusion region other than said groove portion; and

forming a gate electrode on the top surface of said gate insulator film.

12. A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising the steps of:

selectively forming a semiconductor layer on said

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semiconductor substrate;

using the selectively formed semiconductor layer as a mask to diffuse an impurity in the surface of said semiconductor substrate to form an impurity diffusion region including an elevated impurity diffusion region elevated from a channel plane which is formed on the surface of the masked semiconductor substrate;

forming an oxide film on the side of the surface of said elevated impurity diffusion region to use said semiconductor layer as a stopper to polish the surface of said oxide film, and thereafter, removing said semiconductor layer;

forming a gate insulator film of a high dielectric film in a region bordering said elevated impurity diffusion region and said oxide film so that the top surface of said gate insulator film is arranged farther from said substrate than the interface between said impurity diffusion region and said oxide film; and

forming a gate electrode on the top surface of said gate insulator film.

13. A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising the steps of:

selectively depositing semiconductor layers serving as source/drain regions, which sandwich a region serving as a channel plane on said semiconductor substrate therebetween, so that an inclined surface is formed between the top surface of said semiconductor layers and said channel plane;

forming a dummy gate insulator film and a dummy gate electrode including a second semiconductor layer on said channel plane, which borders the selectively formed semiconductor layers, by a technique including at least a lithography;

using said second semiconductor layer as a mask to diffuse an impurity in the surface of said semiconductor substrate to form impurity diffusion regions;

removing said dummy gate electrode, which is formed on a

portion serving as said channel plane sandwiched between said impurity diffusion regions, by etching;

depositing an insulator film of a high dielectric film on the whole surface of the exposed channel plane to form a gate insulator film, which has a cross section of a grooved space at the center thereof; and

depositing a gate electrode on the top surface of said gate insulator film, which is formed on the whole surface so as to have a grooved space at the center thereof, to form a gate electrode having a cross section of a T shape.